

1 In the Claims:

2

3 Please amend Claim 1 as follows.

4

5 1. (Currently Amended) In a target processor, a
6 trace apparatus comprising:

7 a trigger unit responsive to user and target processor
8 state input signals, the trigger unit generating control
9 signals in response to the input signals;

10 timing trace apparatus, the timing trace apparatus
11 responsive to control signals for selectively providing
12 timing trace streams during secondary code execution;

13 ~~program counter/data~~ counter and data trace apparatus,
14 the ~~program counter/data~~ counter and data trace apparatus
15 responsive to signals from the control apparatus for
16 selectively providing ~~program counter/data~~ counter and data
17 trace streams during secondary code execution when the
18 timing trace unit is providing signal during the secondary
19 code execution, and

20 a test and debug port, the test and debug port adapted
21 for coupling to a communication bus, the test and debug
22 port receiving signal from and sending signals to a host
23 processor unit.

24

25 Please amend Claim 2 as follows.

26

27 2. (Currently Amended) The trace apparatus as
28 recited in claim 1 wherein secondary code execution is
29 ~~background/interrupt~~ a background or interrupt service
30 routine code execution.

1 3. **(Original)** The trace apparatus as recited in
2 claim 1 wherein the target processor is can have one of an
3 unprotected pipeline and a protected pipeline.
4

5 4. **(Original)** The trace apparatus as recited in
6 claim 1 further comprising a pipeline flattener, the
7 pipeline flattener aligning the program counter address
8 with the completion of the instruction, the pipeline
9 flattener flushing instructions in response to a halt
10 execution signal in an unprotected pipeline, the pipeline
11 flattener halting operation in a protected pipeline.
12

13 5. **(Original)** The trace apparatus as recited in
14 claim 1 where in the target processor has three states, a
15 primary code execution state, a secondary code execution
16 state, and an execution halt state.
17

18 6. **(Original)** The trace apparatus as recited in
19 claim 5 wherein the timing trace stream can be controllably
20 enabled during an execution halt state.
21

22 **Please amend Claim 7 as follows.**
23

24 7. **(Currently Amended)** A method of ~~controlling~~
25 generating trace streams in a target processor for
26 transmission to a host processor, the method comprising:
27 generating a timing trace stream in the target
28 processor in response to preselected user and target
29 processor input signals; and

1 when the timing trace stream is being generated,
2 generating a program counter and a data trace stream in
3 response to predetermined user and target processor input
4 signals; and
5 sending the trace streams to the host processing unit
6 over a communication bus.

7
8 8. **(Original)** The method as recited in claim 7
9 further comprising including in the target processor input
10 signals indicia of the state of the target processor, the
11 target processor having a primary code execution state, a
12 secondary code execution state and an execution halt state.

13
14 9. **(Original)** The method as recited in claim 7
15 further comprising including in the target processor input
16 signals indicia indicating whether the target processor was
17 in a protected pipeline mode of operation or in an
18 unprotected pipeline mode of operation.

19
20 10. **(Original)** The method as recited in claim 7
21 further comprising including in the user input signals
22 whether the timing trace was enabled during instruction
23 execution halts.

24
25 **Please amend Claim 11 as follows.**

26
27 11. **(Currently Amended)** The method as recited in
28 claim 9 further comprising including in the user input
29 signals identifying when ~~whether~~ the timing trace stream
30 was enabled during the secondary code execution state.

1 Please amend Claim 12 as follows.

2

3 12. (Currently Amended) A processing unit comprising:
4 a central processing unit, the central processing unit
5 having three states of operation, a primary code execution
6 state, a secondary code execution state and an execution
7 halted state; and

8 trace generating apparatus including:

9 a program counter trace stream generation unit,
10 the program counter trace stream generation unit and the
11 data trace generation unit responsive to control signals
12 for generating the program counter and the data trace
13 streams respectively;

14 a timing trace stream generation unit, the timing
15 trace stream generation unit generating a timing trace
16 stream in response to control signals; and

17 a trigger unit responsive to user input signals
18 and to central processing unit signals for generating first
19 and second control signals controlling the timing trace
20 generation unit and the program counter and data trace
21 generation unit; and

22 a port for applying selected trace signals to a
23 communication bus.

24

25 13. (Original) The processing unit as recited in
26 claim 12 wherein first control signals enable the timing
27 trace generation unit during the secondary code execution
28 state.

29

1 14. (Original) The processing unit as recited in
2 claim 13 wherein second control signals enable the timing
3 trace generation device and the program counter and data
4 trace generation units during the secondary code execution.

5
6 15. (Original) The processing unit as recited in
7 claim 12 including indicia of a protected pipeline mode of
8 operation and of an unprotected mode of operation of the
9 central processing unit are part of the central processing
10 unit input signals.